IN THE CLAIMS

Claims 1-16 (canceled).

17.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units operable to execute said plurality of instructions fetched from said memory in parallel;

a first plurality of signal lines for sending data stored in said register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in said register; and

a bypass circuit for connecting said first and second plurality of signal lines to use data resulting from operation by said arithmetic operation unit for a next cycle operation, said bypass circuit being controlled by an instruction executed by said plurality of arithmetic operation units.

18.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units operable to execute different instructions of said plurality of instructions fetched from said memory in parallel;

a first plurality of signal lines connected between outputs of said registers and inputs of said arithmetic operation units;

a second plurality of signal lines connected between outputs of said arithmetic operation units and inputs of said registers; and

a bypass circuit for connecting said first and second plurality of signal lines to use data resulting from operation by an arithmetic operation unit for a next cycle operation, said bypass circuit being controlled by an instruction executed by said plurality of arithmetic operation units.

19. (previously presented) The data processor according to claim 17, wherein said bypass circuit comprises switches for connecting said first and second plurality of signal lines.

20. (previously presented) The data processor according to claim 18, wherein said bypass circuit comprises switches for connecting said first and second plurality of signal lines.

21. (currently amended) A data processor comprising:

a sequencer which causes means for fetching from memory a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

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the plurality of arithmetic operation units operable to execute said plurality of instructions fetched from said memory in parallel;

a first plurality of signal lines for sending data stored in said register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in said register; and

a plurality of switches for connecting said first and second plurality of signal lines to use data resulting from operation by one arithmetic operation unit for operation by another arithmetic operation unit.

22.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units operable to execute different instructions fetched from said memory in parallel;

a first plurality of signal lines, connected between said registers and said arithmetic operation units, for transferring data from a register to an arithmetic operation unit;

a second plurality of signal lines, connected between said arithmetic

operation units and said registers, for transferring data from an arithmetic

operation unit to a register; and

a plurality of switches for connecting said first and second plurality of

signal lines to use data resulting from operation by one arithmetic operation

unit for operation by another arithmetic operation unit.

23. (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality

of instructions at a time to be fetched from memory in one machine cycle, said

plurality of instructions using a plurality of arithmetic operation units;

a register file for storing data; and

the plurality of arithmetic operation units operable to execute

operations based on said instructions fetched from said memory,

wherein said register file has a bypass circuit for transferring data from

an output of a first arithmetic operation unit to an input of a second arithmetic

operation unit in order that a first operation and a second operation are

executed consecutively, and that a result of said first operation is used for

said second operation.

24. (previously presented) The data processor according to

claim 23, wherein said register file has a plurality of registers.

25. (previously presented)   The data processor according to claim 24, wherein said plurality of registers and said plurality of arithmetic operation units are connected with a first plurality of signal lines and a second plurality of signal lines, said first plurality of signal lines sending data stored in a register to an arithmetic operation unit and said second plurality of signal lines sending data resulting from operation by an arithmetic operation unit to a register, and said bypass circuit comprises switches for connecting said first plurality of signal lines and said second plurality of signal lines.

26. (previously presented)   The data processor according to claim 23, wherein said first operation and said second operation are executed by different arithmetic operation units.

27. (currently amended) A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data stored in said register to said arithmetic operation units;

a second plurality of signal lines for storing data resulting from operation by said arithmetic operation units to said register; and

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a bypass circuit for transferring data between different arithmetic

operation units when instructions executed by said different arithmetic

operation units indicate a same register address.

28.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality

of instructions at a time to be fetched from memory in one machine cycle, said

plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units for executing operations

based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data stored in said registers to

said arithmetic operation units;

a second plurality of signal lines for storing data resulting from

operation by said arithmetic operation units to said registers; and

a bypass circuit for transferring data between different arithmetic

operation units when instructions executed by said different arithmetic

operation units indicate a same register address.

29.   (previously presented)   The data processor according to

claim 27, wherein said   instructions are consecutive ones to be executed

by said different arithmetic operation units.

30. (previously presented)   The data processor according to claim 28, wherein said   instructions are consecutive ones to be executed by said different arithmetic operation units.

31. (currently amended)A data processor comprising:

a sequencer which causes means for fetching from memory a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data from said register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in said register; and

a plurality of switches for connecting said first and second plurality of signal lines to transfer data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

32. (currently amended)A data processor comprising:

a sequencer which causes means for fetching from memory a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

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the plurality of arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

a first plurality of signal lines for sending data from a register to an arithmetic operation unit;

a second plurality of signal lines for storing data resulting from operation by an arithmetic operation unit in a register; and

a plurality of switches for connecting said first and second plurality of signal lines to transfer data between different arithmetic operation units when instructions executed by said different arithmetic operation units indicate a same register address.

33.   (previously presented)   The data processor according to claim 31, wherein said   instructions are consecutive ones to be executed by said different arithmetic operation units.

34.   (previously presented) The data processor according to claim 32, wherein said   instructions are consecutive ones to be executed by said different arithmetic operation units.

35.   (currently amended)A data processor comprising:

a sequencer which causes means for fetching from memory a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a register for storing data;

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the plurality of arithmetic operation units operable to execute said plurality of instructions fetched from said memory in parallel;

a first group of signal lines for sending data stored in said register to said plurality of arithmetic operation units;

a second group of signal lines for storing data resulting from operation by said arithmetic operation units to said register; and

a bypass circuit for connecting said first group of signal lines and said second group of signal lines,

wherein data resulting from operation by an arithmetic operation unit is not only stored in said register, but also sent to another arithmetic operation unit through said bypass circuit.

36.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using a plurality of arithmetic operation units;

a plurality of registers for storing data;

the plurality of arithmetic operation units operable to execute said plurality of instructions fetched from said memory in parallel;

a first plurality of signal lines, connected to said registers and said arithmetic operation units, for transferring data from a register to an arithmetic operation unit;

a second plurality of signal lines, connected to said arithmetic operation units and said registers, for transferring data from an arithmetic operation unit to a register; and

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a bypass circuit for transferring data from said second plurality of signal lines to said first plurality of signal lines,

wherein storing data resulting from operation by an arithmetic operation unit and transferring the data to another arithmetic operation unit are executed in a same cycle.

37.   (currently amended)A data processor comprising:

a sequencer which causes ~~means for fetching from memory~~ a plurality of instructions at a time to be fetched from memory in one machine cycle, said plurality of instructions using first and second arithmetic operation units;

a plurality of registers;

the first and second arithmetic operation units for executing operations based on said plurality of instructions fetched from said memory;

first signal lines for transferring data from said registers to said first arithmetic operation unit;

second signal lines for transferring data from said registers to said second arithmetic operation unit;

third signal lines for transferring data from said first arithmetic operation unit to said registers;

fourth signal lines for transferring data from said second arithmetic operation unit to said registers;

a first bypass circuit for transferring data from said third signal lines to said second signal lines; and

a second bypass circuit for transferring data from said fourth signal lines to said first signal lines.

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38.   (previously presented)   The data processor according to claim 35, wherein said bypass circuits comprise switches.

39.   (previously presented)   The data processor according to claim 36, wherein said bypass circuits comprise switches.

40.   (previously presented)   The data processor according to claim 37, wherein said bypass circuits comprise switches.